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In the United States Patent and Trademark Office

Serial number 09/340,172
Application filed June 25, 1999
Applicant Derek Wong
Application Title Methods for Increasing Instruction-Level Parallelism in Microprocessors and Digital Systems
Examiner/GAU Eric Coleman / 2183

Mailed December 22, 2003
at San Jose, California

From:
Derek Wong
1341 Echo Valley Dr.
San Jose, CA 95120

To:
Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, DC 20231

RE: Amendment C to patent application 09/340,172

Thank you for reviewing patent application 09/340,172.

In response to the office action letter regarding patent application 09/340,172 mailed on August 21, 2003, the applicant encloses a substitute specification in clean and marked form and this letter.

Also enclosed are an IDS submission and an amended set of claims for submission.

The amended set of claims has only two changes: claim 44 has been amended with an additional limitation and claim 87 is new.

The figure numbers in the specification have been corrected, and revised headings have been placed into the document as suggested in the office action. Also, the section ordering has been changed as suggested. (The marked form of the substitute specification shows inserted material

in underline as well as italics (e.g. *inserted words*). This is the way that the word processor (Lotus WordPro) used by the applicant marks inserts.)

Most of the references in the IDS are for background information.

The applicant has amended claim 44 with an additional limitation as follows:

> "wherein said instruction stream cache comprises means of storing and later fetching a transformed code block that spans more than one cache line in said instruction stream cache."

This is intended to further enhance the limitations in claim 44 to strongly distinguish the claimed invention over certain IDS references. Neither Johnson (IDS reference 6) nor Rotenberg et al (IDS references 7 and 8) provide a mechanism for transforming or storing code blocks that are longer than one cache line or VLIW cache entry. Johnson also does not have any regular cache. An important feature in the present patent application is the means to transform a longer code block and then store the transformed code block in the instruction stream cache as a group of cache lines. This storage is accomplished using data structures such as hyperblock ID tags and line numbers or pointers to chain together multiple cache lines into one hyperblock, as described on pages 19-22 of the patent application. Johnson and Rotenberg et al (references 6-8 in the IDS) do not have an equivalent mechanism for managing longer code blocks, nor do they emphasize the idea that transforming longer code blocks would be advantageous.

Beyond this distinction, the proposed designs in Johnson and Rotenberg et al are in-order instruction packing mechanisms and are much more simple than the present application's design. The designs in Johnson and Rotenberg perform no instruction re-ordering, no predication, nor other operations.

The applicant would also like to respectfully submit claim 87 as a new dependent claim dependent on claim 44 which contains a further description of the means to handle code blocks that span multiple cache lines. (Because claim 86 was previously cancelled in amendment B, the total number of claims does not increase from the original patent application submission.)

The applicant respectfully submits the amended claim set and suggests that amended claim 44 and new claim 87 should be allowable over the prior art.

Note on claim 77: Reference 13 in the IDS by Wang and Franklin does not describe any structure like in claim 44 of the present application. Therefore, dependent claim 77 should be allowable over IDS reference 13.

The applicant has reviewed the references cited in previous office actions. These references do not appear to describe the presently claimed inventions and do not appear render the claimed inventions to be obvious in any way.

The applicant is available at telephone number 408-927-7940 to discuss this application.

Thank you for your review of this application and thank you for your help.

Very respectfully,

Derek Wong

Derek Wong

Patent Applicant

Express Mail Label # EU727223990US Date of Deposit December 22, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service using "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to "Assistant Commissioner for Patents, Washington, DC 20231."

Signed Derek Wong Inventor